In the Claims:

Claims 1 and 2 are canceled.

3. (Previously Presented) A method of fabricating a semiconductor device, comprising:

providing a layer of high-k dielectric material over a substrate;

providing a layer of conductive material over the high-k dielectric layer;

patterning the conductive layer;

providing spacers along sidewalls of the patterned conductive layer;

performing a first etch on the high-k dielectric layer, wherein a portion of the high-k dielectric layer being etched with the first etch remains after the first etch; and

performing a second etch of the high-k dielectric layer to remove at least part of the remaining portion of the high-k dielectric layer, wherein the second etch differs from the first etch, wherein the first and second etches of the high-k dielectric layer are performed, at least in part, in alignment with the spacers.

4. (Previously Presented) The method of claim 3, wherein the first etch is a dry etch process.

5. (Original) The method of claim 4, wherein the dry etch process is a reactive ion etching process using an etch chemistry comprising at least one of inert gas, chlorine, and fluorine.

6. (Previously Presented) The method of claim 3, wherein the second etch is a wet etch process.

7. (Original) The method of claim 6, wherein the wet etch process uses an etch chemistry comprising an inorganic acid.

8 (Original) The method of claim 7, wherein the inorganic acid comprises at least one of a halogen acid, HF, and H_2SO_4.

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9. (Previously Presented) A method of fabricating a semiconductor device, comprising:

providing a layer of high-k dielectric material over a substrate;

providing a layer of conductive material over the high-k dielectric layer;

patterning the conductive layer;

performing a first etch on the high-k dielectric layer, wherein a portion of the high-k dielectric layer being etched with the first etch remains after the first etch; and

performing a second etch of the high-k dielectric layer to remove at least part of the remaining portion of the high-k dielectric layer, wherein the second etch differs from the first etch, wherein the patterning of the conductive layer, the first etch, and the second etch are performed in a same chamber.

10. **Cancel**

11. (Previously Presented) The method of claim 3, wherein the high-k dielectric material comprises at least one of an aluminum oxide, a zirconium oxide, a hafnium oxide, a hafnium silicate, a zirconium silicate, a silicon nitride, a tantalum oxide, a barium strontium titanate, and a lead-lanthanum-zirconium-titanate.

12. (Previously Presented) A method of fabricating a semiconductor device, comprising:

providing a layer of high-k dielectric material over a substrate;

providing a layer of conductive material over the high-k dielectric layer;

patterning the conductive layer;

performing a first etch on the high-k dielectric layer, wherein a portion of the high-k dielectric layer being etched with the first etch remains after the first etch;

changing material properties of the remaining portion of the high-k dielectric layer during the first etch; and

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performing a second etch of the high-k dielectric layer to remove at least part of the remaining portion of the high-k dielectric layer, wherein the second etch differs from the first etch.

13. (Previously Presented) The method of claim 3, wherein the high-k dielectric layer is provided using a process selected from a group consisting of chemical vapor deposition, metal-organic chemical vapor deposition, atomic layer deposition, atomic layer chemical vapor deposition, low pressure chemical vapor deposition, sputtering, and anodization.

14. (Previously Presented) The method of claim 3, wherein the high-k dielectric layer has an initial thickness prior to the first etch, wherein the remaining portion of the high-k dielectric layer has a first thickness after the first etch, the first thickness being about half the initial thickness.

Claims 15-22 are cancelled.

23. (Previously Presented) The method of claim 9, wherein the first and second etches of the high-k dielectric layer are performed in alignment with the patterned conductive layer.

24. (Previously Presented) The method of claim 9, wherein the first etch is a dry etch process.

25. (Previously Presented) The method of claim 9, wherein the second etch is a wet etch process.

26. Cancel

27. (Previously Presented) The method of claim 9, further comprising:

changing material properties of the remaining portion of the high-k dielectric layer during the first etch.

28. Cancel

29. Cancel

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30. Cancel

31. Cancel

32. Cancel

33. (Previously Presented) The method of claim 12, wherein the first and second etches of the high-k dielectric layer are performed in alignment with the patterned conductive layer.

34. (Previously Presented) The method of claim 12, wherein the first etch is a dry etch process.

35. (Previously Presented) The method of claim 12, wherein the second etch is a wet etch process.

36. (Previously Presented) The method of claim 12, wherein the patterning of the conductive layer, the first etch, and the second etch are performed in a same chamber.

37. Cancel

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